CLAIMS

1. In a semiconductor die having an op-amp, a method of reducing package stress, which comprises the act of:

placing matched components of the op-amp substantially in a region of the die having the least stress gradients.

2. The method according to clam 1, wherein the region is substantially in the center of the die.

3. The method according to clam 2, wherein the center is the common centroid of the die.

4. The method according to clam 1, wherein the matched components are current mirror input stages of the op-amp.

5. The method according to clam 1, wherein the op-amp is one of a single, dual, and quad op-amp.

6. The method according to clam 1, wherein the op-amp is a differential op-amp.

7. The method according to clam 1, which further comprises:

disposing the matched components away from the periphery of the die.

8. The method according to clam 1, which further comprises:

disposing gain stages of the op-amp in an intermediate region of the die.

9. The method according to clam 1, which further comprises:

disposing output stages of the op-amp in an outer region of the die.

10. In a semiconductor die having an op-amp, a method of reducing variance of an input offset voltage, which comprises the act of:

reducing package stress by placing matched components

of the op-amp substantially in a region of the die having the least stress gradients.

11. The method according to clam 10, wherein the region is substantially in the center of the die.

12. The method according to clam 11, wherein the center is the common centroid of the die.

13. In a semiconductor die having an op-amp, a method of reducing trim circuitry, which comprises the act of:

reducing variance of an input offset voltage of the op-amp by placing matched components of the op-amp substantially in a region of the die having the least stress gradients.

14. A semiconductor configuration, comprising:

a die having a region with the least stress gradients and an op-amp, said op-amp containing matched components substantially in said region.

15. The semiconductor configuration according to clam 14, wherein said region is substantially in the center of the die.

16. The semiconductor configuration according to clam 15, wherein the center is common centroid of the die.

17. The semiconductor configuration according to clam 14, wherein said matched components are current mirror input stages.

18. The semiconductor configuration according to clam 14, wherein said op-amp is one of a single, dual, and quad op-amp.

19. The semiconductor configuration according to clam 14, wherein said die includes an intermediate region having gain stages.

20. The semiconductor configuration according to clam 14, wherein said die includes an outer region having output stages.